REMARKS

Reconsideration of this application is respectfully requested in view of the [the following remarks.

Claims 1 and 4 are withdrawn from examination. Therefore, Claims 2-3 and 5-6 are currently pending in the application and subject to examination. In the Office Action mailed November 8, 2005, the Examiner rejected claims 2 and 5 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,311,234 to Seshan et al. ("Seshan"). The Examiner rejected claims 3 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Seshan in view of U.S. Patent No. 5,640,598 to Sato ("Sato") and further in view of JP Patent No. 02195464 A to Hoshino ("Hoshino").

The Applicant hereby traverses the rejections, as follows.

I. Claims 2 and 5

Claims 2 and 5 recite in part a DMA controller comprising a setting register . . . an operation register . . . an operation controller . . .and a transfer executer. The Applicants submit that Seshan does not teach the claimed elements comprised within the DMA controller of claims 2 and 5. Seshan teaches the DMA (143) controlled by and configured by several memory mapped control registers. (See Figures 1B and 4 and Column 6, Line 43). These controllers are mapped into the CPU's (10) memory space, and include the DMA Global Data Registers. (See Column 7, Lines 59-67).

Moreover, Seshan teaches that "Some of the DMA control register can be pre-loaded for the next block transfer through reload registers. Selected DMA Global Data registers act as the reload registers." (See Column 11, Lines 18-21). This statement in Seshan referring to the DMA Global Data Registers as registers within the CPU,

describes the operation of the registers within a CPU, rather than the configuration of registers or counters within a DMA controller.

The operation register and other elements recited in claims 2 and 5 are registers and other elements provided within a DMA controller, separate from the memory space of a CPU. Therefore, the Applicants submit that Seshan does not disclose or suggest the DMA controller recited in claims 2 and 5.

Moreover, the DMA controller in claims 2 and 5 includes in part a transfer executer for executing DMA transfers based on the data stored in the operation register or the operation counter. Seshan merely teaches, as discussed above, that the DMA controller is so configured as to be pre-loadable. The Applicants submit that Seshan does not disclose or suggest the DMA controller comprising a transfer executer for executing DMA transfers based on the data stored in an operation register or operation counter.

Therefore, the Applicants submit that claims 2 and 5 are allowable over the cited prior art for at least these reasons.

II. Claims 3 and 6

The Applicants respectfully traverse the rejections of claim 3 and 6. Claims 3 and 6 recite in part a DMA controller comprising a setting register for storing transfer conditions under which DMA transfer is to be executed next time, a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register, a selector for alternatively selecting one of the setting register and the setting execution register, and a selection controller for performing control so that the register selected by the

selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends. As discussed above, the Applicants assert that Seshan does not disclose or suggest at least the claimed registers, including the setting register, provided within a DMA controller.

Sato does not cure the deficiency in Seshan. Furthermore, the rejection relies on Sato as teaching a setting register for storing transfer conditions under which DMA transfer is currently being executed and a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register.

The Applicants submit that Sato does not teach at least a setting register for storing transfer conditions under which DMA transfer is to be executed next time. Sato teaches SA6, DA7, and TC8 functioning in the DMA controller as operation registers for storing transfer conditions under which the DMA transfer is currently being executed. (See Figure 1 (40), Figure 7 and Column 4 Lines 34-67). Sato teaches the DMA controller further provided with SAΦ50, DAΦ51, and TCΦ52. (See Figure 1). However, as shown in Figure 6 and 7, SAΦ50, DAΦ51, and TCΦ52 are exclusively for the initial setting of the DMA transfer not for storing transfer conditions under which DMA transfer is to be executed next time.

Even assuming that Sato disclosed such a setting register, Sato does not disclose or suggest a setting execution register, as claimed in claims 3 and 6. Sato merely teaches "when DMA transfer is executed, the program of the procedure performed by the DMA controller is stored in the DMA controller." (See Column 6, Lines

9-27). The program storing area 22 for storing the program in Sato is utterly different from the setting execution register as claimed in claims 3 and 6.

Therefore, even if Seshan and Sato were combined (not admitted) they do not teach the limitations of claims 3 and 6.

Hoshino does not cure the deficiency in either Seshan or Sato. Furthermore, the rejection relies on Hoshino as teaching a selector for alternatively selecting one of the setting register and the setting execution register and a selection controller for performing control for that, when DMA transfer is started, data stored in the register is written to the operation register. The Applicants respectfully submit that Hoshino does not disclose or suggest at least a selector for alternatively selecting one of the setting register or a setting execution register as claimed in claims 3 and 6. Hoshino merely teaches that "on completion of DMA transfer under certain transfer conditions, other transfer conditions are selected by a selector, and DMA transfer is executed under those other transfer conditions." (See abstract). The operation of Hoshino is different from the operation of switching the register selected by the selector alternately between the setting register and the setting execution register every time that the DMA transfer ends, as claimed in claims 3 and 6.

Therefore, the Applicants submit that even if Seshan, Sato, and Hoshino were combined (not admitted) the combination does not teach the limitations of claims 3 and 6. The Applicants assert, for at least these reasons, that claims 3 and 6 are allowable over the cited prior art.

With regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of

obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

In the Office Action, the Examiner merely states that the present invention is obvious in light of the cited references. See, e.g., Office Action at pages 5 and 6. This is an insufficient showing of motivation.

CONCLUSION

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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